PACKAGE ENCAPSULATION
DESIGN RULES & GUIDELINES

Samtec Microelectronics Group provides extensive advanced package design and assembly capabilities as well as the ability to assist in choosing the best technology and materials for your specific application.

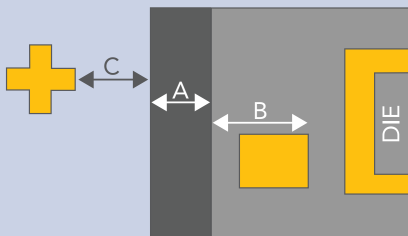
In addition to substrate and package design, flip chip, die attach, wirebond and sealing, our capabilities also include thermal management, wafer dicing, lid attach and marking. Visit www.samtecmicroelectronics.com for additional information.

The following dimensions are guidelines designed to help release product to manufacturing as quickly as possible. Full capabilities are not limited to the specifications included in this document. Please contact SME@samtec.com for applications with tighter requirements.

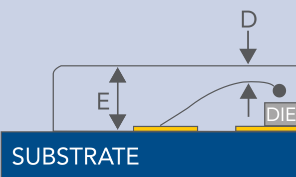
TYPICAL STRUCTURE & SPECIFICATIONS FOR PACKAGE ENCAPSULATION

- Maximum encapsulation thickness (board surface to top of encapsulation): 0.024" (600)
- Automated dispense tool heated work area: 12" x 16"
- Total work area: 20" x 30"
- Machine positioning accuracy and repeatability: +/- 0.001"

TOP DOWN



SIDE PROFILE



TYPICAL PACKAGE DESIGN RULES

	DESCRIPTION	ORGANIC (min) INCHES (µm)
A	Dam Width	0.012" (300)
B	Space of Dam to Wirebond Lead Edge	0.012" (300)
C	Space of Fiducial to Dam*	0.007" (175)
D	Overlap of Encapsulation to Top of Wirebond Loop	0.007" (175)
E	Height of Encapsulation**	= A / 2

*Must be outside encapsulated region
**Board surface to top of encapsulation

For more IC Packaging solutions, please visit www.samtecmicroelectronics.com or contact SME@samtec.com.

© 2016 SAMTEC, INC. SEPTEMBER 2016