FINE PITCH WIREBOND
DESIGN RULES & GUIDELINES

Samtec Microelectronics Group provides extensive advanced package design and assembly capabilities as well as the ability to assist in choosing the best technology and materials for your specific application.

In addition to substrate and package design, flip chip, die attach, wirebond and sealing, our capabilities also include thermal management, wafer dicing, lid attach and marking. Visit www.samtecmicroelectronics.com for additional information.

The following dimensions are guidelines designed to help release product to manufacturing as quickly as possible. Full capabilities are not limited to the specifications included in this document. Please contact SME@samtec.com for applications with tighter requirements.

TYPICAL STRUCTURE & SPECIFICATIONS FOR WIRING & SUBSTRATE PAD DESIGN

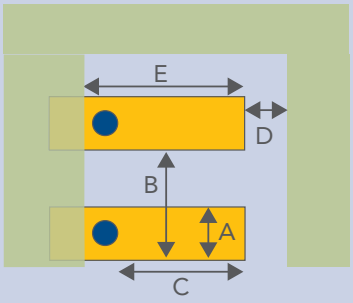
Plating and layout requirements for substrate pad design as well as wire parameters:

- Wedge Bond - ENIG plating is acceptable; typical wire types include Al, Au and Pt
- Ball Bond - ENEPIG plating is recommended; typical wire types include Au and Cu

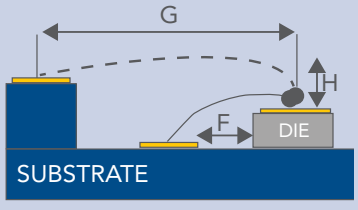
Processes that use Au ball bond, require Gold plate per MIL-G–45204, Type III, Grade A, Class 1:

- 99.9% purity minimum
- < 90 Knoop hardness
- 50 µ" thick, minimum

TOP DOWN



SIDE PROFILE



TYPICAL WIREBOND SPECIFICATIONS

	DESCRIPTION	ORGANIC (min) INCHES (µm)	CERAMIC (min) INCHES (µm)
A	Wirebond Pad	0.004" (100)	0.003" (75)
B	Wirebond Pad Pitch	0.008" (200)	0.006" (150)
C	Overlap of Wirebond Lead Edge to Via	0.008" (200)	0.007" (175)
D	Space Solder Mask to Wirebond Lead Edge	0.004" (100)	-
E	Overlap of Wirebond Lead Edge to Solder Mask	0.008" (200)	-
F	Space of Die Edge to Wirebond Lead Edge*	0.015" (375) or 2x Die Thickness (whichever is greater)	
G	Maximum Wire Length	0.250" (6350)	
H	Maximum Wire Height	0.100" (2540)	

*Assumes no ground plane for die attach

For more IC Packaging solutions, please visit www.samtecmicroelectronics.com or contact SME@samtec.com.